PCIe/PXIe-5411

High Speed Digital I/O Module

User Manual

User Manual Version: V1.8.5

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Table of Contents

1. Introduction

This chapter presents the information how to use this manual and operate the module if you are already familiar with Microsoft Visual Studio and C# programming language.

1.1 Overview

The PCIe / PXIe-5411 is a high speed digital I/O (HSDIO) module, which can be run on various buses including PCIe, PXIe, TXI (based on thunderbolt 3) and USB (to be released). PCIe / PXIe-5411 provides 32 channels of configurable digital input and output, and the main parameters are shown in Table 1 below.

Number of DIO channels	32 configurable I / O per channel
Voltage Level	1.8 V, 2.5 V, 3.3 V, 5 V
DI sample rate (MS / s)	50
DO update rate (MS / s)	50
Signal type	single-ended
Maximum frequency of sampling clock	50 MHz
Maximum available clock frequency	200 MHz

Table 1 PCIe /PXIe-5411 products Main Features

1.1.1 Product Function Overview

PCIe/PXIe-5411 is a 32 channels high speed digital I/O (HSDIO) module. The direction of all the 32 digital channels can be programmed by software.. The signal level supports 4 options: 1.8V, 2.5V, 3.3V and 5V. Data sequence can be modified by software. The device utilizes a high-throughput PCI Express bus and multi-core optimized drivers and application software to provide high-performance capabilities.

1.1.2 Product Uses

High speed digital waveform I / O: parallel high speed digital input or output data stream with hardware timing.

Static digital signal input / output: Software digital input status polling, or digital output status setting.

1.2 Main features

- 32CH high speed DIO
- 8CH multipurpose PFI
- Maximum clock rate 50MHz
- Independent data direction control of each channel
- Support voltage level: 1.8v/2.5v/3.3v/5v
- 128M sampe point cache
- High performance TCXO clock on board
- 2CH clock generator for sampling clock

1.3 Abbreviation

DI: Digital Input

DO: Digital Output

DAQ: Data AcQuisition

PFI: Programmable Function Interface

PLL: Phase Locked Loop

TXCO: Temperature Compensate X'tal (crystal) Oscillator

1.4 Learn by Example

JYTEK has added **Learn by Example** in this manual. We provide many sample programs for this device. Please download and install the sample programs for this device. You can download a JYPEDIA excel file from our web www.jytek.com. Open JYPEDIA and search for JY5411 in the driver sheet, select **JY5411_Examples.zip**. This will lead you to download the sample program for this device. In addition to the download information, JYPEDIA also has a lot of other valuable information, JYTEK highly recommend you use this file to obtain information from JYTEK.

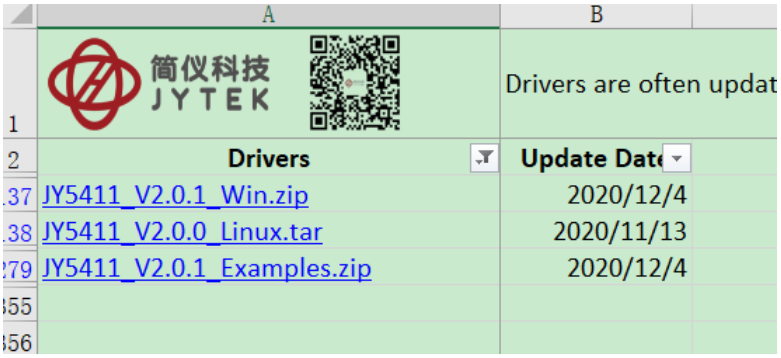

Figure 1

In a **Learn by Example** section, the sample program is in bold style such as **Digital Input--> Winform DI Continuous;** the property name in the sample program is also in bold style such as **SamplesToAcquire**; the technical names used in the manual is in italic style such as *SampleRate*. You can easily relate the property names in the example program with the manual documentation.

In an Learn by Example section, the experiment is set up as follow. One PCIe/PXIe-5411 card is plugged in a desktop computer. The PCIe/PXIe-5411 is connected to a DIN-68H-01 terminal block through a cable with 50- ohm impedance. A signal source is also connected to the same terminal block.

Tip: PCIe/PXIe-5411 also has the digital output capability. If you do not have a signal source, you can use the digital output of PCIe/PXIe-5411 as the signal source. In this case you need first run example program ***Digital Output-->Winform DO Continuous Wrapping Multichannels*** *to generate the output signal.*

2. Hardware Specifications

2.1 System Diagram

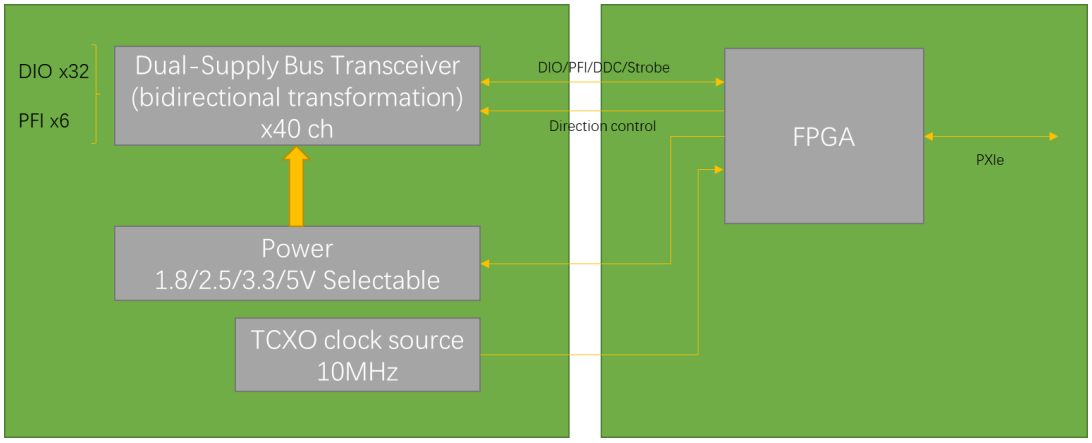

Figure 2 PCIe/PXIe-5411 System Block Diagram

Figure 2 shows the system architecture of PCIe/PXIe-5411. The system is mainly composed of front panel interface, dual supply bus transceiver, power, clock source and FPGA control module. The power supply module level standard can be 1.8V/2.5V/3.3V/5V, clock source is supported by PXIe-CLK100, PXIe-SYNC100, 25MHz onboard, PXI_TRIG (0 ~ 7), PXI_STAR, etc. It mainly realizes the function of high-speed digital input and output.

2.2 Hardware Specification

2.2.1 Basic

DIO

Number of Channels	32
DIO Direction Control	Per Channel
Synchronous Acquisition	Yes
Support Function	Continuous Waveform / Software Single Point
DI FIFO	64 MSamples
DO FIFO	64 MSamples
Level Standard	1.8 V/2.5 V/3.3 V/5 V Level (Software Selection)

PFI

Number of Channels	8
PFI Direction Control	Per Channel

Clock

Number of Clock Input Terminals	8 (Using PFI<0..7>)
Number of Clock Output Terminals	8 (Using PFI<0..7>)

Table 2 Basic Specification

2.2.2 Waveform Acquisition（DI）

Basic

Digital Input	DIO<0..31>
Signal Type	Single Ended
Input Impedance	2.5 MΩ
Input Protection Range	-0.5 V ~ 6.5 V
Max DI Sampling Rate	50 MHz

Voltage Levels

Logic Level	Max Low Input Level	Min High Input Level
1.8 V	0.65 V	1.2 V
2.5 V	0.7 V	1.7 V
3.3 V	0.8 V	2 V
5 V	1.5 V	3.5 V

Table 3 Waveform Acquisition (DI) Sepcification

2.2.3 Waveform Generation（DO）

Basic

Digital Output	DIO<0..31>
Signal Type	Single Ended
Typical Output Impedance	50 Ω
Enable/Disable Control	Per Channel
Output Protection Range	-0.5 V ~ (UserVcc + 0.5 V)
Output Protection Duration	No Duration
Max DO Update Rate	50 MHz

Voltage Levels

Logic Level	Typical Low Level	Maximum Low Level	Typical High Level	Minimum High Level
1.8 V	0 V	0.1 V	1.8 V	1.7 V
2.5 V	0 V	0.1 V	2.5 V	2.4 V
3.3 V	0 V	0.1 V	3.3 V	3.2 V
5 V	0 V	0.1 V	5 V	4.85 V

DC Drive Capability

Maximum DC Drive Capability(1.8 V)	4 mA
Maximum DC Drive Capability(2.5 V)	8 mA
Maximum DC Drive Capability(3.3 V)	24 mA
Maximum DC Drive Capability(5 V)	32 mA

Table 4 Waveform Generation (DO) Sepcification

2.2.4 Waveform Characteristics

Memory and Scripting

Maximum Onboard Memory Size	64 MSamples DI + 64 MSamples DO
Waveform Quantum	1 Sample
Acquisition Minimum Record Size	1 Sample
Acquisition Record Quantum	1 Sample
Acquisition Total Pre-Reference Trigger Samples	0 ~ Full record
Acquisition Total Post-Reference Trigger Samples	0 ~ Full record

Trigger

Trigger Mode	StartTrigger ReferenceTrigger (DI only) ReTrigger (DI only)
Trigger Source	PFI<0..7> PXI_Trig<0..7> Software
Generation Minimum Required Trigger Pulse Width	20 ns
Acquisition Minimum Required Trigger Pulse Width	20 ns
ReTrigger Rearm Time	2 Samples MAX
Delay From Trigger to Digital Data Output	1 Sample

Miscellaneous

Warm-Up Time:	15 min
Onboard Clock Accuracy:	±0.3 ppm
Onboard Clock Stability:	±2.5 ppb
Onboard Clock Aging:	±4.6 ppm (in 20 years)

Table 5 Waveform Characteristics

2.2.5 Timing Characteristics

Sampling Clock Source	Internal Clock
	PXIe_SYNC100
	PFI<0..7>
	PXIe_DSTAR A/B
	PXIStar
	PXI Trigger
Timebase	200 MHz
Onboard TCXO	10 MHz
Sampling Clock Frequency Range(PFI)	8 Hz-50 MHz
Sampling Clock Frequency Range(PXI_Star)	8 Hz-50 MHz
Sampling Clock Frequency Range(PXIe_DSTAR)	8 Hz-50 MHz
Sampling Clock Frequency Range(PXI Trigger)	8 Hz-20 MHz

PLL

PLL Input Source	PXIe_CLK100 PXI_DSTARA On board TCXO
PLL output routing	DI or DO sample clock
Typical PLL Lock time	2000 ms
PLL Frequency	100-200 MHz
Duty Cycle	50%

Table 6 Timing Characteristics

2.2.6 Physical and Environment

Bus

PXIe Standard	x8 PXIe Peripheral Module Specification V1.0 Compliant
Slot Supported	x1 and x4 PXI Express, PXI Express hybrid, or PXI Express System Timing Slot

Power

3.3 V:	TBD
+12 V:	TBD

Size

External physical size	3 U PXIE
Weight	185g

Environment

Operating temperature	0 ~ 50 ℃

Table 7 Physical and Environment Specification

2.3 Front Panel and Pin Definition

The interface description of the front panel of the board is shown in Figure 3 below:

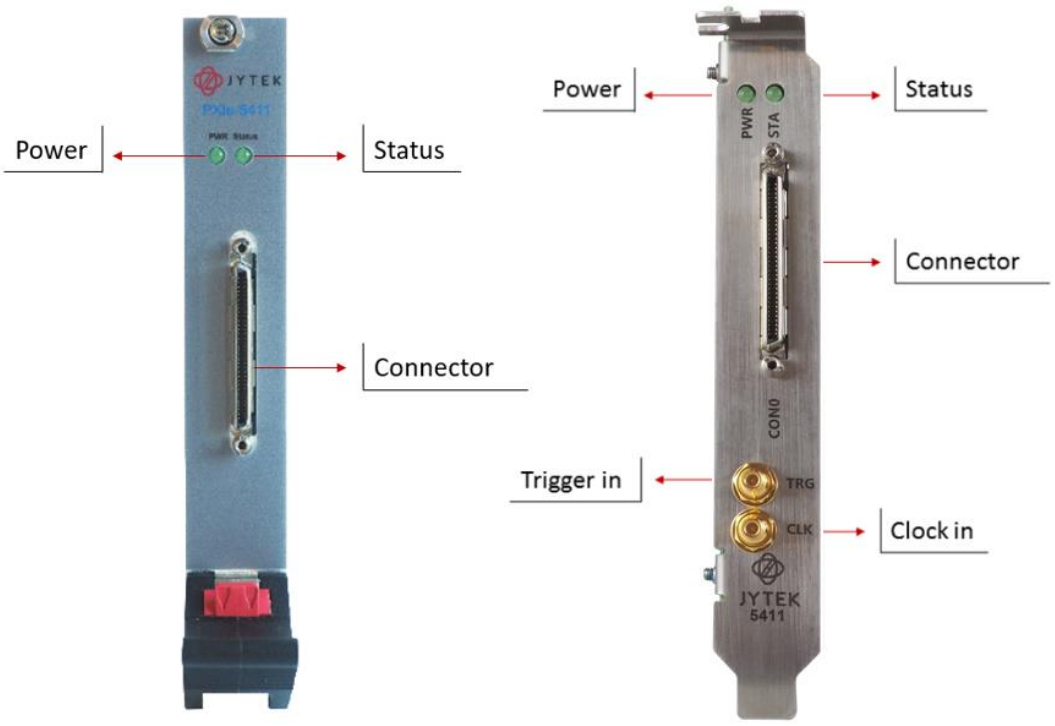

Figure 3 PCIe / PXIe-5411 front panel

The definition and description of PCIe / PXIe-5411 outgoing line are shown in Table 8 and Table 9

SCSI-VHDCI 68pin			
Signal name	pin	pin	Signal name
DIO30	35	1	DIO31
GND	36	2	GND
DIO28	37	3	DIO29
GND	38	4	GND
DIO26	39	5	DIO27
GND	40	6	GND
DIO24	41	7	DIO25
GND	42	8	PFI0
DIO22	43	9	DIO23
GND	44	10	GND
DIO20	45	11	DIO21
GND	46	12	GND
DIO18	47	13	DIO19
GND	48	14	GND
DIO16	49	15	DIO17
GND	50	16	GND
DIO14	51	17	DIO15
PFI1	52	18	GND
DIO12	53	19	DIO13
GND	54	20	GND
DIO10	55	21	DIO11
GND	56	22	GND
DIO8	57	23	DIO9
GND	58	24	GND
DIO6	59	25	DIO7
PFI3	60	26	PFI2
DIO4	61	27	DIO5
GND	62	28	GND
DIO2	63	29	DIO3
PFI5	64	30	PFI4
DIO0	65	31	DIO1
GND	66	32	GND
PFI7	67	33	PFI6
GND	68	34	GND

Table 8 definition of PCIe / PXIe-5411 pin diagram

Signal name	Signal definition
DIO<0..31>	Digital I / O channel
PFI<0..7>	programmable function port
GND	digital signal reference

Table 9 definition and description of signal

3. Software

3.1 System Requirements

PCIe/PXIe-5411 can be used in a Windows or a Linux operating system.

Microsoft Windows: Windows 7 32/64 bit, Windows 10 32/64 bit.

Linux Kernel Versions: There are many Linux versions. It is not possible JYTEK can support and test our devices under all different Linux versions. JYTEK will at the best support the following Linux versions.

Linux Version
Ubuntu LTS
16.04： 4.4.0-21-generic(desktop/server)
16.04.6：4.15.0-45-generic(desktop) 4.4.0-142-generic(server)
18.04： 4.15.0-20-generic(desktop) 4.15.0-91-generic(server)
18.04.4：5.3.0-28-generic (desktop) 4.15.0-91-generic(server)
Localized Chinese Version
中标麒麟桌面操作系统软件（兆芯版）V7.0（Build61）: 3.10.0-862.9.1.nd7.zx.18.x86_64
中标麒麟高级服务器操作系统软件V7.0U6: 3.10.0-957.el7.x86_64

Table 10 Supported Linux Versions

3.2 System Software

When using the PCIe/PXIe-5411 in the Windows environment, you need to install the following software from Microsoft website:

Microsoft Visual Studio Version 2015 or above,

.NET Framework version is 4.0 or above.

.NET Framework is coming with Windows 10. For Windows 7, please check .NET Framework version and upgrade to 4.0 or later version.

Given the limited resources, JYTEK only tested PCIe/PXIe-5411 with .NET Framework 4.0 and Microsoft Visual Studio 2015. JYTEK relies on Microsoft to maintain the compatibility for the newer versions.

3.3 C# Programming Language

The default programming language of all the examples provided by JYTEK is Microsoft C#. This is Microsoft's recommended programming language in Microsoft Visual Studio and is particularly suitable for the test and measurement applications. C# is also a cross-platform programming language.

3.4 PCIe/PXIe-5411 Series Hardware Driver

After installing the required application development environment as described above, you need to install the PCIe/PXIe-5411 hardware driver.

JYTEK hardware driver has two parts: the shared common driver kernel software (FirmDrive) and the specific hardware driver.

Common Driver Kernel Software (FirmDrive): FirmDrive is the kernel software for all hardware products of JYTEK. You need to install the FirmDrive software before using any other JYTEK hardware products. FirmDrive only needs to be installed once. After that, you can install the specific hardware driver.

Specific Hardware Driver: Each JYTEK hardware has a specific C# hardware driver. This driver provides rich and easy-to-use C# interfaces for users to operate various PCIe/PXIe-5411 functions. JYTEK has standardized the ways which JYTEK and other vendor's DAQ boards are used by providing a consistent user interface, methods, properties and enumerations in the object-oriented programming environment. Once you get yourself familiar with how one JYTEK DAQ card works, you should be able to know how to use all other DAQ hardware by using the same methods.

3.5 Install the SeeSharpTools from JYTEK

To efficiently and effectively use PCIe/PXIe-5411, you need to install a set of free C# utilities, SeeSharpTools from JYTEK. The SeeSharpTools offer rich user interface functions that you will find convenient in developing your applications. They are also needed to run the examples that come with PCIe/PXIe-5411 hardware. Please register and down load the latest SeeSharpTools from our website, www.jytek.com.

3.6 Running C# Programs in Linux

Most C# written programs in Windows can be run by MonoDevelop development system in a Linux environment. You would develop your C# application in Windows using Microsoft Visual Studio. Once it is done, run this application in the MonoDevelop

environment. This is JYTEK's recommended way to run your C# programs in a Linux environment.

If you want to use your own Linux development system other than MonoDevelop, you can do it by using our Linux driver. However, JYTEK does not have the capability to support the Linux applications. JYTEK completely relies upon Microsoft to maintain the cross-platform compatibility between Windows and Linux using MonoDevelop.

4. Operating PCIe/PXIe-5411

This chapter mainly introduces the related operation guide of PCIe / PXIe-5411, mainly including the definition and usage of driver. The function introduction includes static DI/ DO and dynamic DI/ DO.

JYTEK provides a large number of exsamples, online help and documents to help you use the PCIe / PXIe-5411. We strongly recommend that you read these examples before writing your own application. In many cases, the examples can also help a lot of actual test projects start quickly.

4.1 Quick Start

After you have installed the driver software and the SeeSharpTools, you are ready to use Microsoft Visual Studio C# to operate the PCIe/PXIe-5411.

If you are already familiar with Microsoft Visual Studio C#, the quickest way to use PCIe/PXIe-5411 is to go through our extensive examples. We provide source code of our examples. In many cases, you can modify the source code and start to write your applications.

4.2 Programmable Multifunctional I / O

PCIe / PXIe-5411 supports powerful programmable I / O functions and 32 channels of DI / DO. For more information, refer to examples.

4.2.1 Static DI/ DO Loopback

Programmable I/O function supports static digital input and output with 32 channels. User canaccess the I / O information through software polling.

Learn by Example 4.2.1

- Connect PCIe/PXIe-5411 DIO30 (Pin#35) to DIO31 (Pin#1).
- Open **Multi Function-->Winform DIO Single.**
- Select **line30** for **Digital Output**, **line31** for **Digital Input** as shown, and click **Start** and **Get Task Status**. The result is shown below.

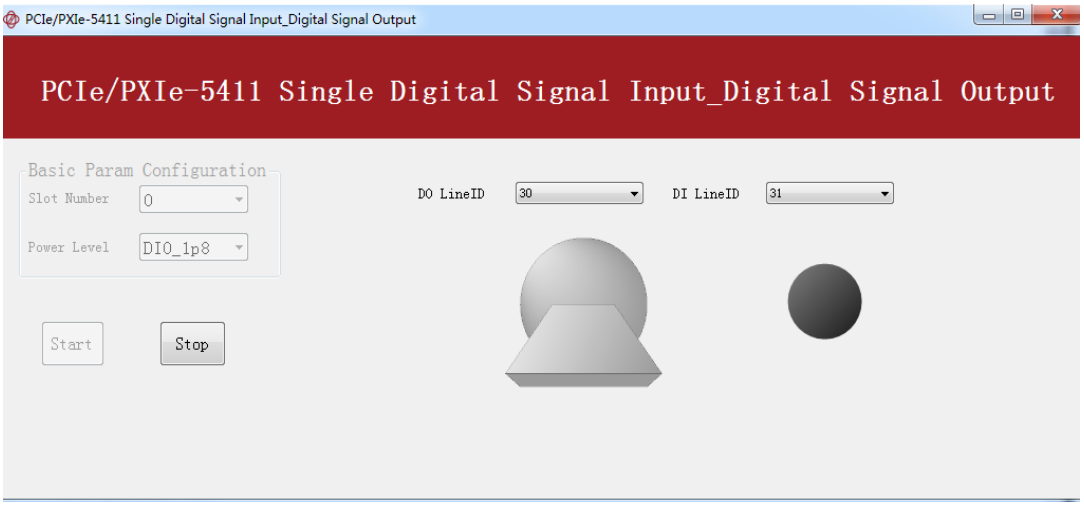

Figure 4

- When the switch line30 in the Digital Output example is “on”, the LED line31 in the Digital Output example will also be “on”.

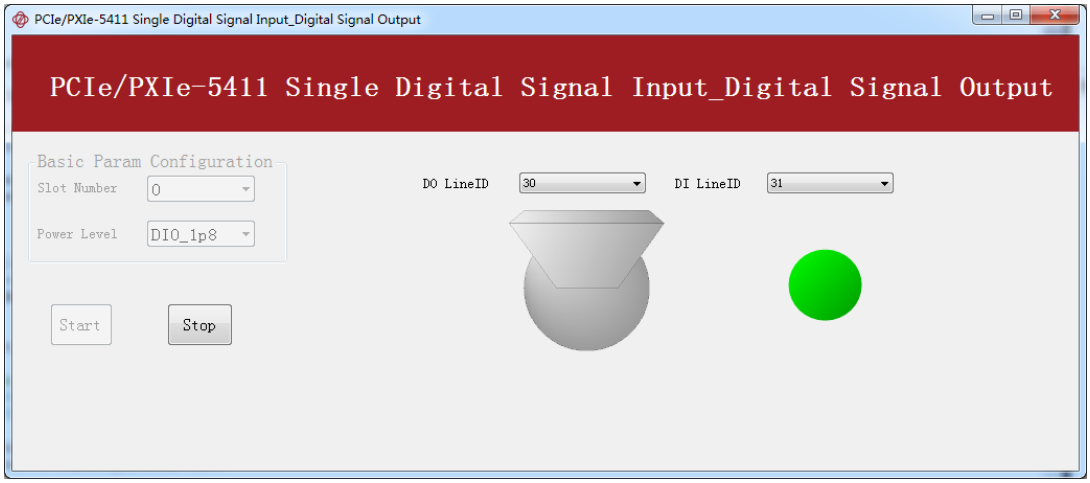

Figure 5

4.2.2 Dynamic DI/ DO Loopback

PCIe / PXIe-5411 supports dynamic DI / DO operation, with a maximum sampling rate of 50MHz and a maximum update rate of 50MHz. User can acquire or generate digital waveforms in this way.

Learn by Example 4.2.2

- Connect PCIe/PXIe-5411 DIO30 (Pin#35) to DIO31 (Pin#1).

- Open **Digital Output--> Winform DO Continuous Wrapping** and **Digital Input-->Winform DI Continuous**
- Select **Channel Number 30** for digital output, **31** for digital input as shown, set the following numbers as shown, and click **Start** in both programs. The result is shown below.

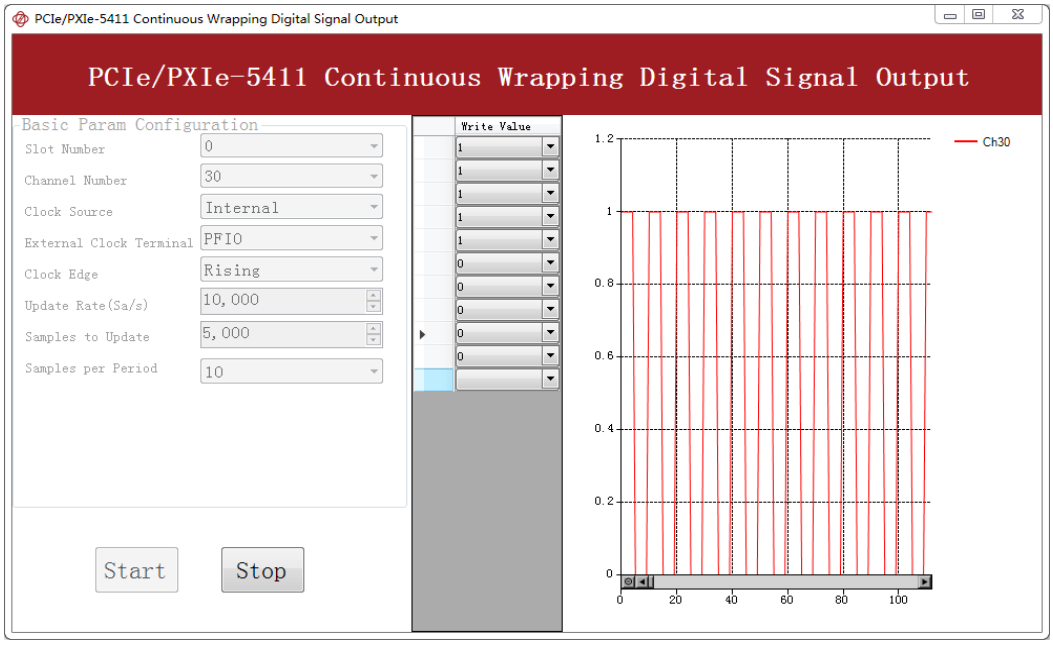

Figure 6

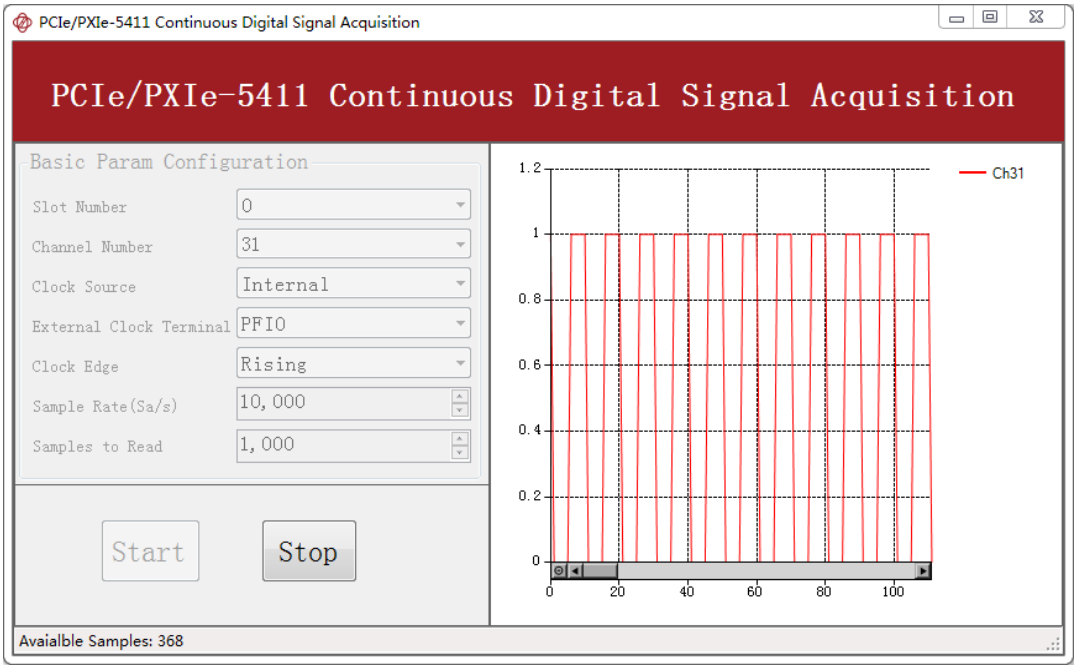

Figure 7

4.2.3 Hardware Timing High-Speed Input Function

After user configures the sampling parameters, the acquired data will be srored to the on-board DDR memory. User can read the collected data through the driver interface and use it for data analysis. You can refer to the examples.

In the DI acquisition mode, user need to configure the acquisition channel and other parameters through the software of PCIe / PXIe-5411. The most important parameters: sampling rate, acquisition channel and acquisition mode:

Sampling Rate: defines the speed of acquisition per second for each channel.

Acquisition Channel: defines the physical channels to acquire signals.

Acquisition Mode: Finite and Continuous.

a) Finite

Finite mode begins data acquisition after DI is started, stops until acquired data length is enough.

b) Continuous

After DI is started, board starts to acquire data until the user sends a stop command.

Once the sampling rate is set, the actual hardware sampling rate is affected by internal clock or external clock source. The sampling clock source is also configured by software. Figure 8 below shows the DI acquisition sequence diagram.

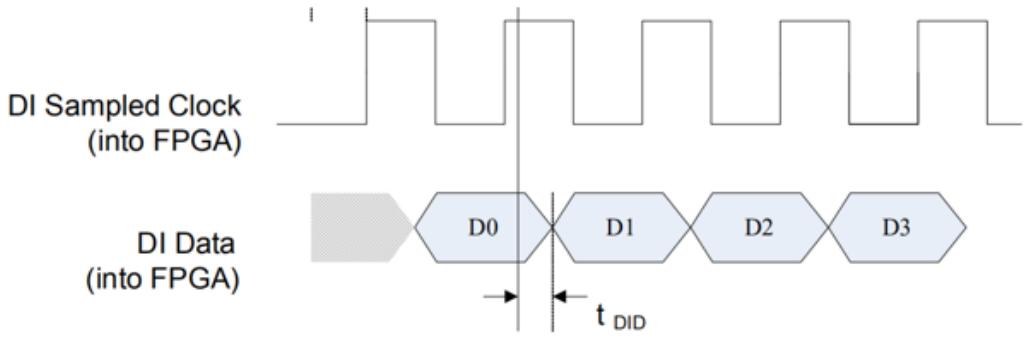

Figure 8 PCIe / PXIe-5411 DI acquisition sequence diagram

Learn by Example 4.2.3

- Connect the signal source's positive output to PCIe/PXIe-5411 DIO0 (Pin#65) and DIO30 (Pin #35) , the negative terminal to the ground GND (Pin#36).
- Set the signal source to generatea squarewave signal (f=5Hz, V_H=5v, V_L=0v).
- Open **Digital Input --> Winform DI Continuous MultiChannels**, set the following parameters as shown. This sample program will continuously acquire data from multiple channels.

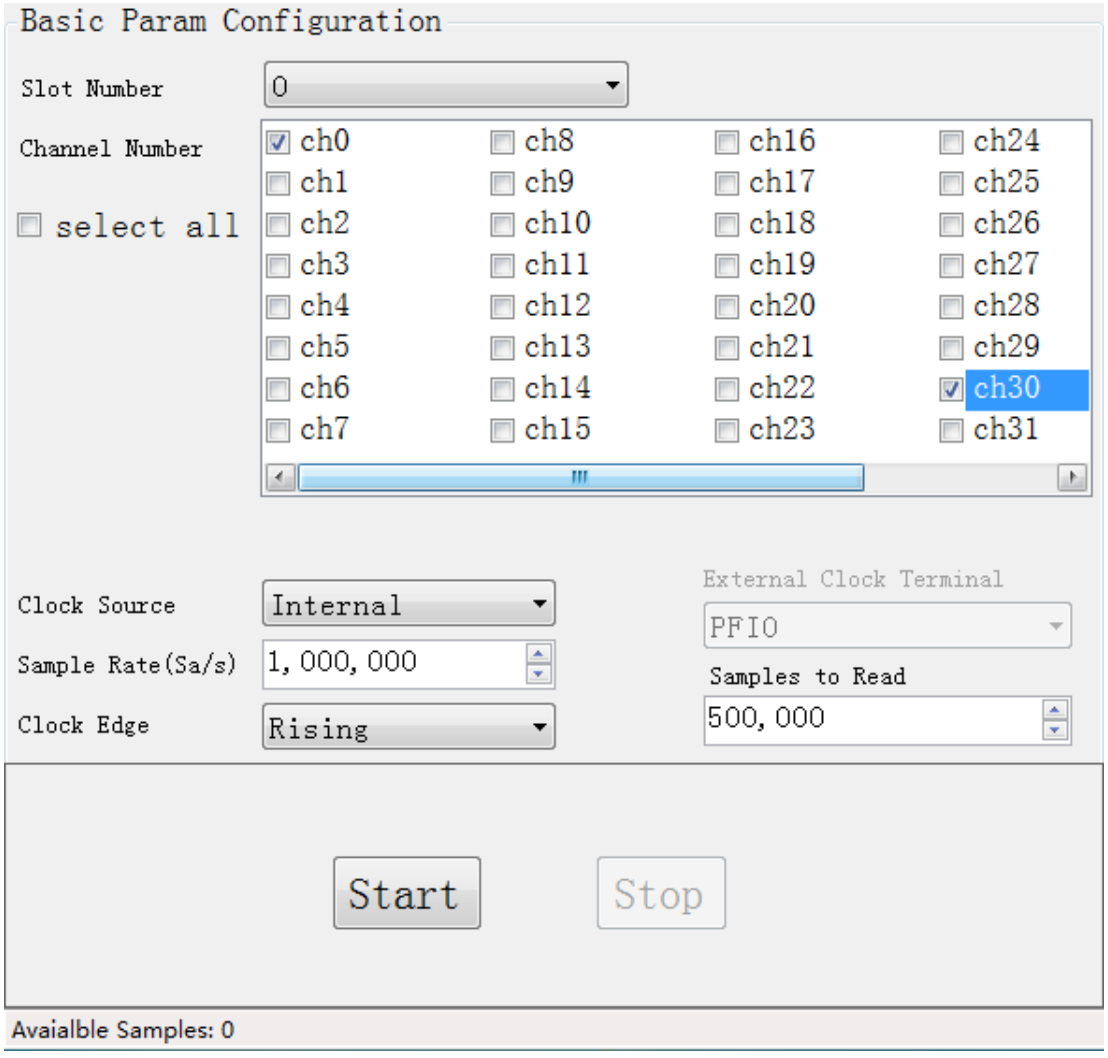

Figure 9

- *SampleRate* is set by **Sample Rate.**
- **Samples to Read** is the total samples to be acquired for each channel in one block. The continuous mode will acquire data blocks after blocks until **Stop** button is pressed.

■ Click **start**, which starts the acquisition. The result is shown below.

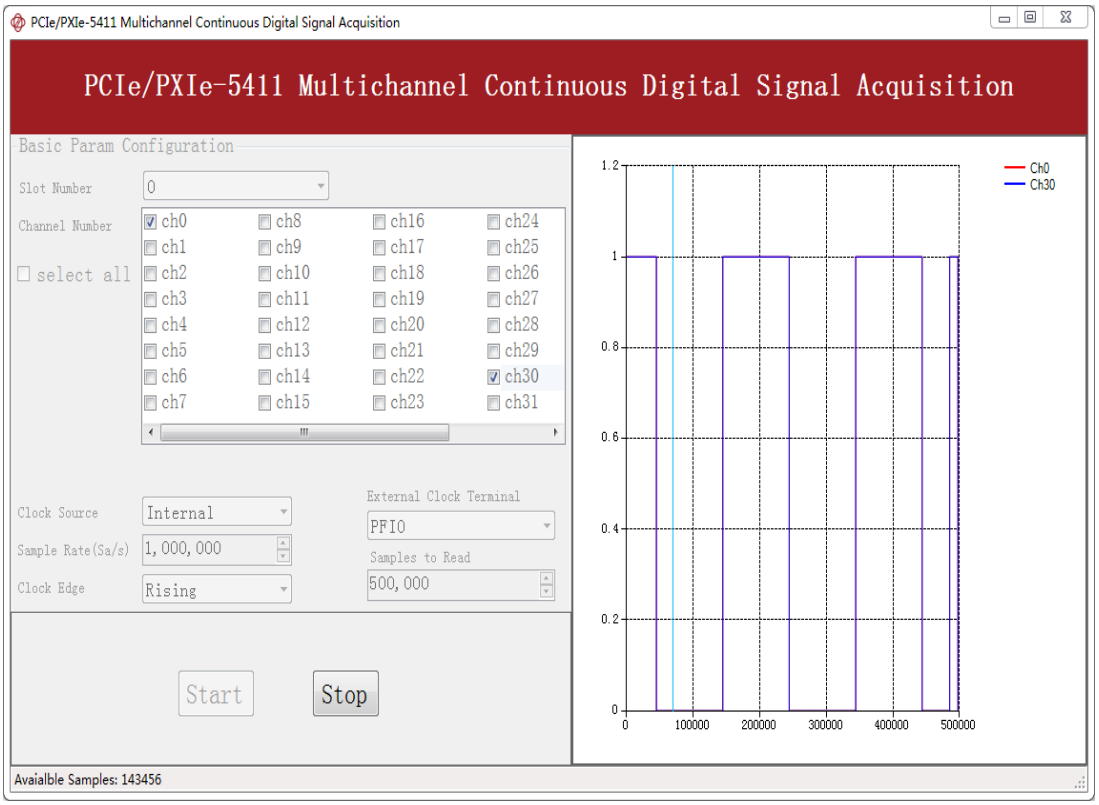

Figure 10

4.2.4 Hardware Timing High-Speed Output Function

The hardware timing high-speed output function of PCIe / PXIe-5411 provides 32 channels of synchronous output, with the maximum update rate of 50MHz; the output level is 1.8V, 2.5V, 3.3V, 5V optional. For more information, see the provided software example.

There are three working modes of digital output:

Finite, ContinuousWraping and ContinuousNoWraping

a) Finite

Finite mode requires the user to write a piece of data. After the DO starts, the program will automatically stop until all the data has been output.

b) ContinuousWraping

The ContinuousWraping mode requiresuser to write a piece of data before starting DO. After DO starts, the board will repeatedly output this piece of data until user the send a stop command.

c) ContinuousNoWraping

The ContinuousWraping mode requires the user to write a piece of data before the starting DO. After DO starts, user needs to write new data to ensure the continuous output of the DO until the user sends a stop command.

Learn by Example 4.2.4

- Open **Digital Output --> Winform DO Continuous NoWrapping MultiChannel,** set the following numbers as shown

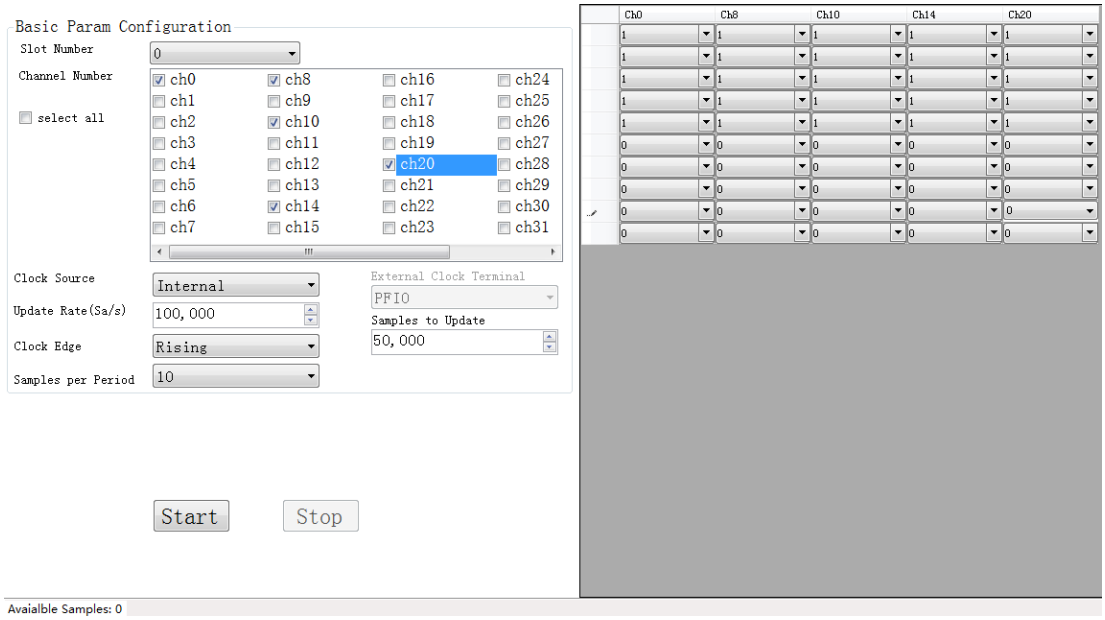

Figure 11

- *Update Rate* is set by **Update Rate**
- **Samples to Update** is the samples to be fenerated for each channel in one block. The continuous mode will output blocks after blocks until **Stop** button is pressed.
- Click **Start.**

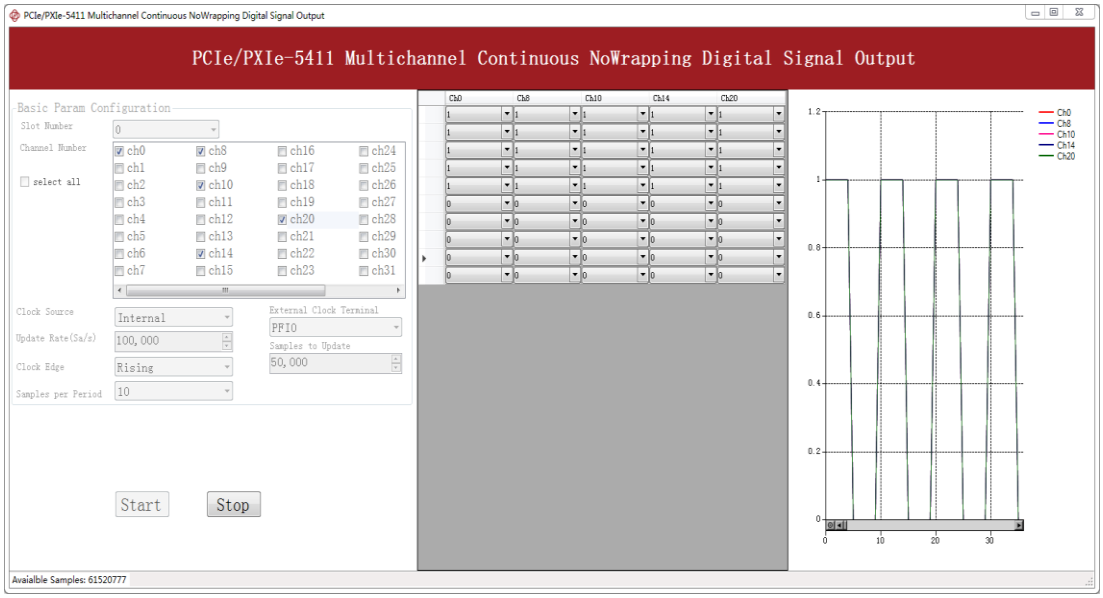

Figure 12

- In **NoWrapping Output** the output wave type can be updated by changing the logic value in **Write Value**.

4.3 Sampling Clock

The sampling clock source has two options: internal and external. The internal clock can reach 200M at most. The optional external clock and the maximum frequency that can be achieved are shown in Table 11

External Clock Source	Maximum frequency
PXIe _Sync100	10 MHz
PXIe_DStarA\PXIe_DStarB	50 MHz
PXI_Star	25 MHz
PXI_Trig<0..7>	10 MHz
PFI<0..7>	50 MHz

Table 11 PCIe / PXIe-5411 optional external clock and maximum achievable frequency

4.4 PLL

PLL (phase locked loop) is a phase-locked clock generator, which can generate clock signal of specified frequency according to the selected time base.

Using on-board TCXO as PLL input source helps to improve PLL output clock performance, including improving clock accuracy, temperature stability and phase noise.

PLL Input source	PXIe_CLK100
	PXI_DSTARA
	TCXO
Typical PLL lock time	2000 ms
Output range	100 MHz ~ 200 MHz

Table 12 PCIe / PXIe-5411 PLL input source

4.5 Trigger Type

PCIe / PXIe-5411 supports three trigger types: immediate trigger, software trigger and external digital trigger. The trigger type is a property set by the driver software. For more information, see the provided software example.

4.5.1 Immediate Trigger

This trigger mode does not require configuration and is triggered immediately when an operation starts. For more information, see the provided software example.

Learn by Example 4.5.1

- Connect the signal source's positive output to PCIe/PXIe-5411 DIO30 (Pin#35), the negative terminal to the ground GND (Pin#36).
- Set a squarewave signal (f=5Hz, V_H=5v, V_L=0v).
- Open **Digital Input --> Winform DI Continuous MultiChannels**, set the following numbers as shown. This sample program will continuously acquire data from multiple channels.

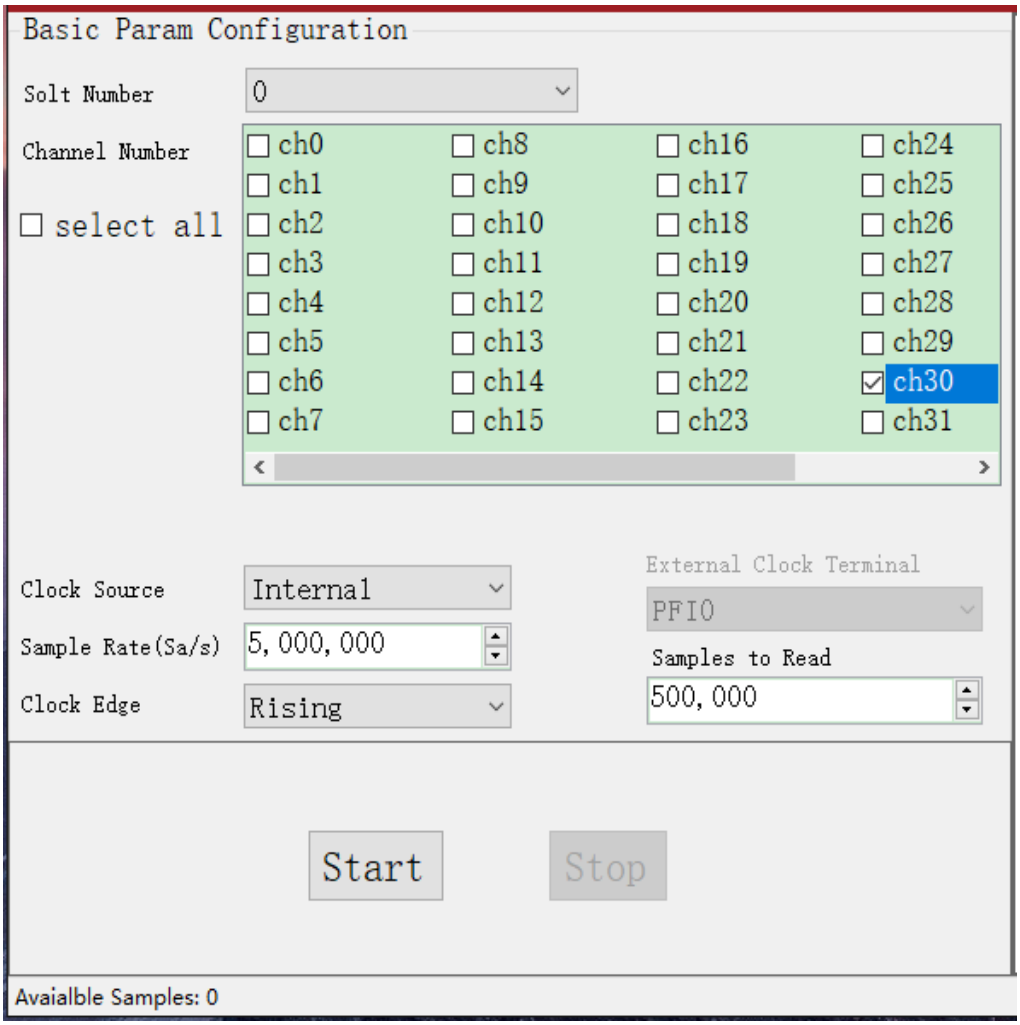

Figure 13

➢ With *Immediate trigger* you can click **Start** to generate the task instead of sending a trigger signal.

4.5.2 Software trigger

Software trigger must be configured by the driver software. The trigger starts when a trigger software routine is being called. For more information, see the provided software example.

Learn by Example 4.5.2

- Connect the signal source positive output to PCIe/PXIe-5411 DIO30 (Pin#35), the negative terminal to the ground GND (Pin#36).
- Set a squarewave signal (f=4Hz, V_H=5v, V_L=0v).
- Open **Digital Input --> Winform DI Continuous Soft Trigger**, set the following parameters as shown.
- Click **Start** to run the task.

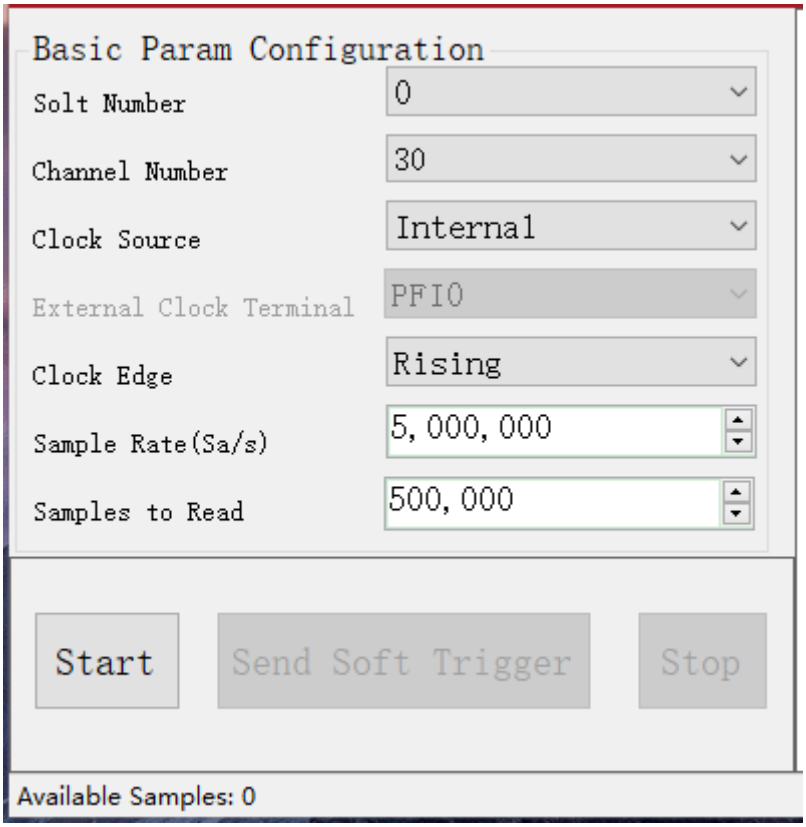

Figure 14

➢ Data will not be acquired until there is a positive signal from *Software Trigger* when **Send Soft Trigger** is clicked.

- After sending the trigger signal, the result will be like this:

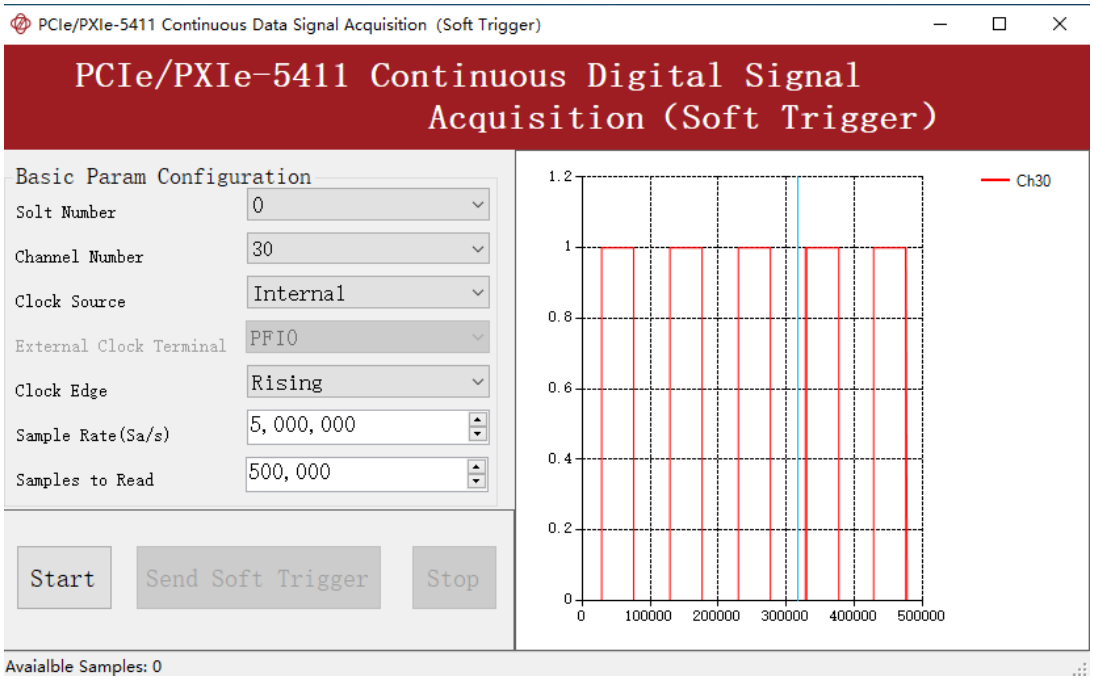

Figure 15

4.5.3 External Digital Trigger

An external digital trigger is generated when the external trigger source pin detects a rising or falling edge. The pulse width of digital trigger shall not be less than 20ns. User can configure the conditions triggered by the software. As shown in Figure 16 Please see the provided software examples for more information.

Figure 16 External Digital Trigger

Learn by Example 4.5.3

- Connect the signal source's positive output to PCIe/PXIe-5411 DIO30 (Pin#35) and digital trigger source (PFI0, Pin#67), the negative terminal to the ground GND (Pin#36). (PFI0, GND) provides the trigger signal.

- Set a squarewave signal (f=5Hz, V_H=5v, V_L=0v).
- Open **Digital Input --> Winform DI Continuous Digital Trigger**, set the following numbers as shown.

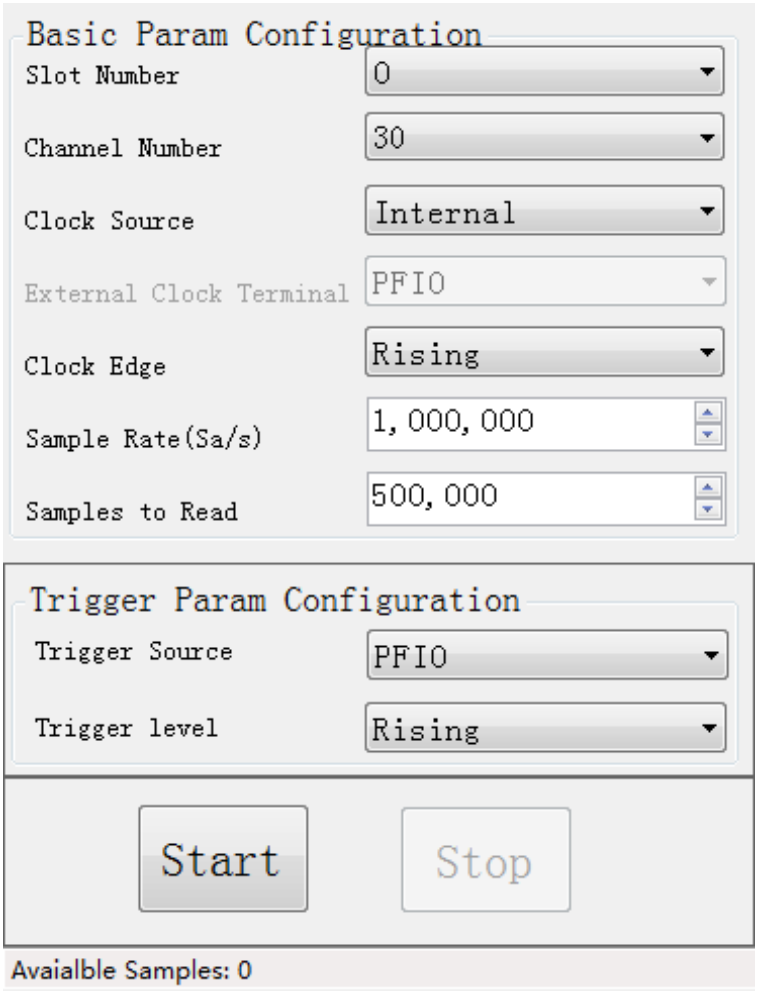

Figure 17

➢ **Trigger Source** must match the pin on PCIe/PXIe-5411.

➢ There are two **Trigger Level**: **Rising** and **Falling.**

- Click **Start** and the result shows below:

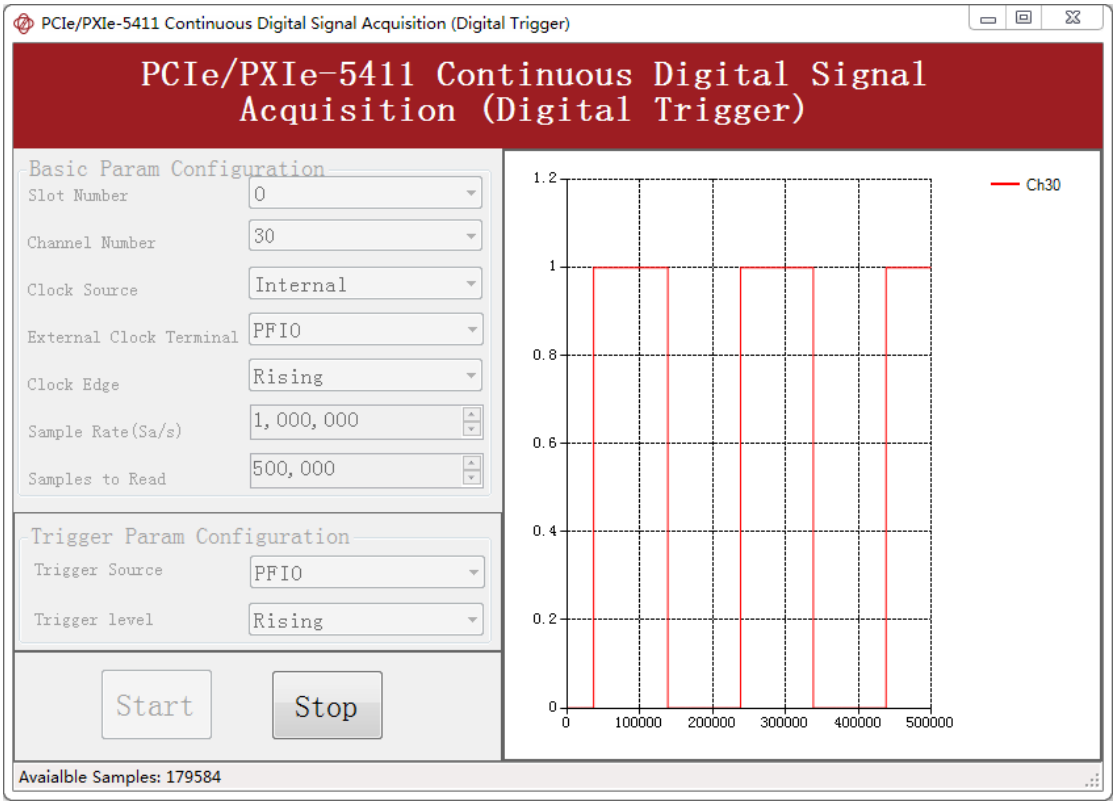

Figure 18

➢ Since The squarewave is used for the digital trigger source, when a rising edge of the squarewave occurs, the digital trigger will be activated, and the data acquisition will start.

4.6 Trigger Mode

The PCIe/PXIe-5411 supports several trigger modes: start trigger, reference trigger, and re-trigger. Please see the provided software examples for more information.

4.6.1 Start Trigger

In this mode, data acquisition begins immediately after the trigger. This trigger mode is suitable for continuous acquisition and finite acquisition. As shown in Figure 19. Please see the provided software examples for more information.

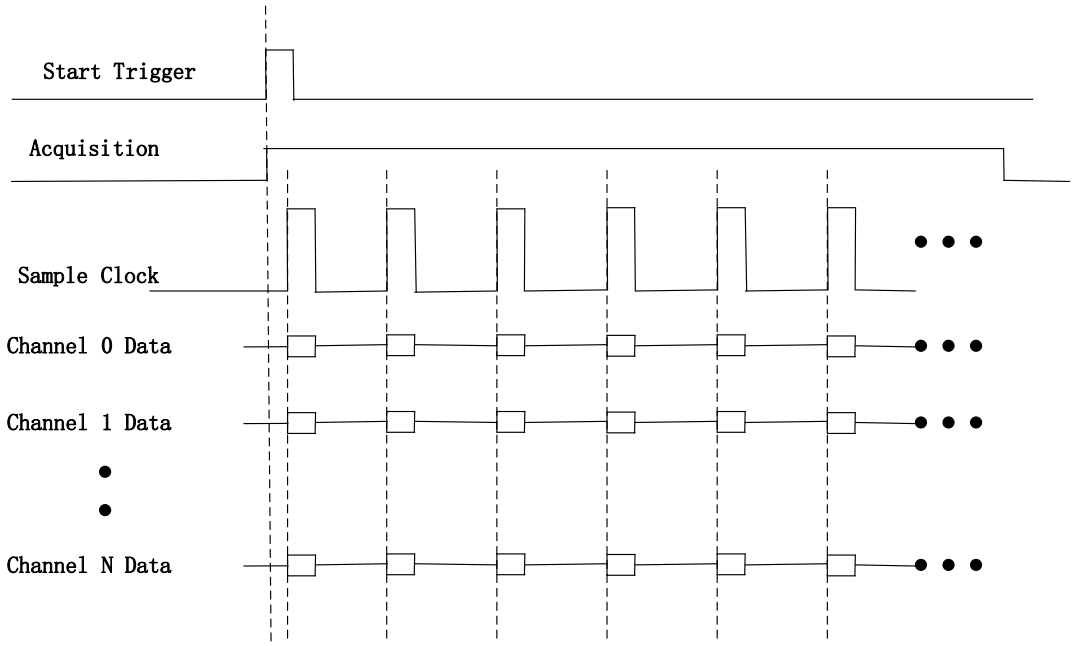

Figure 19 Start Trigger

4.6.2 Reference Trigger

This trigger mode is suitable for finite acquisition. The technique used on a measurement device to keep a circular buffer filled with samples, so that when the reference trigger conditions are met, the buffer includes samples leading up to the trigger condition as well as samples acquired immediately after the trigger. In this mode, user can set the number of pre-trigger samples, which means data acquired before the occurrence of the reference trigger. The default number of pre-trigger points is 0. First you need to start the data acquisition. When the reference trigger condition is met, the driver will return the acquired data points. If the number of

returned points is less than the pre-trigger samples, the trigger signal will be ignored. An example is show below.

Example

- Total samples: 1000;
- Channel Count: 1
- Pre-trigger samples: 10;
- After triggering, it returns total 1000 samples, 10 being pre-triggered, 990 after triggering

The principle is shown in Figure 20. Please see the provided software examples for more information.

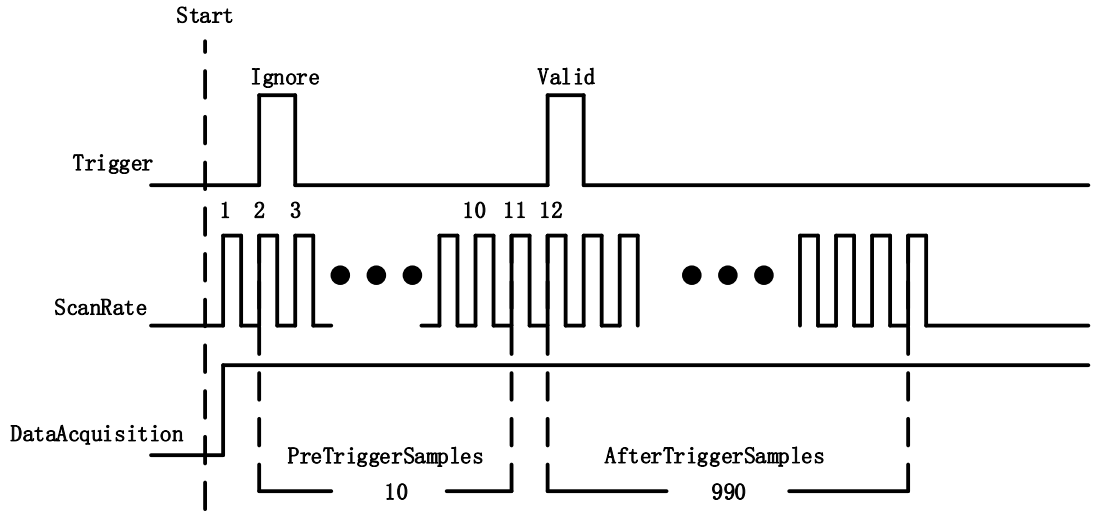

Figure 20 Reference Trigger

4.6.3 ReTrigger

PCIe/PXIe-5411 supports retrigger mode. In the retrigger mode, you can set the number of retriggers and the length of each acquisition. Assuming that the number of re triggers is n and the length of each trigger acquisition is m, the length of all acquisition data is n * m * channelcount, as show in Figure 21.

There are two types of retrigger acquisition, namely finite and infinite. When the number of retriggers is - 1, it is infinite acquisition.

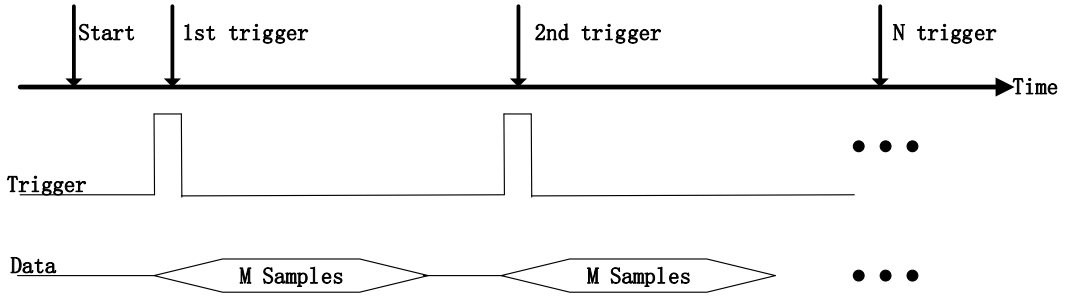

Figure 21 ReTrigger

Learn by Example 4.6

- Connect the signal source's positive output to PCIe/PXIe-5411 DIO30 (Pin#35) and digital trigger source (PFI6, Pin#33). The negative terminal to the ground GND (Pin#36). (PFI6, GND) provides the trigger signal.
- Set a squarewave signal (f=5Hz, V_H=5v, V_L=0v).
- Open **Digital Input-->Winform DI Finite Digital Trigger**, set the following parameters as shown.

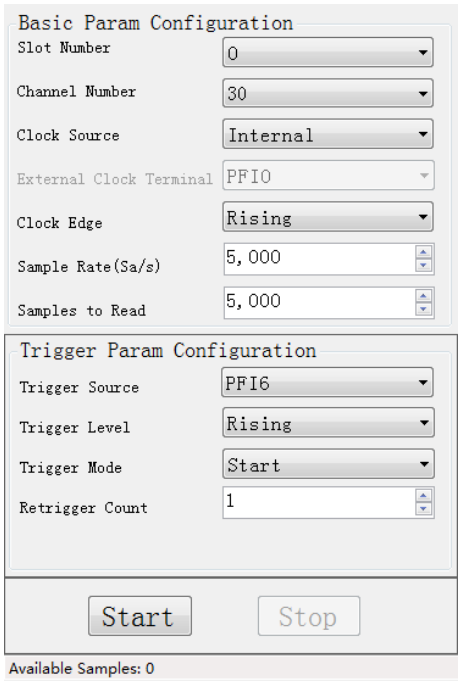

Figure 22

- You can use three different kinds of triggers in this program as mentioned in ***4.6.*** *Start Trigger* and *Reference Trigger* can be set by **Trigger Mode**. *Re-Trigger* can be used by changing the numbers in **Retrigger Count.**

- *pre-trigger samples* are set by **PretriggerSamples**.

- Now the **Trigger Mode** is "**Start**". Click **Start** to begin the data acquisition, the result is shown below:

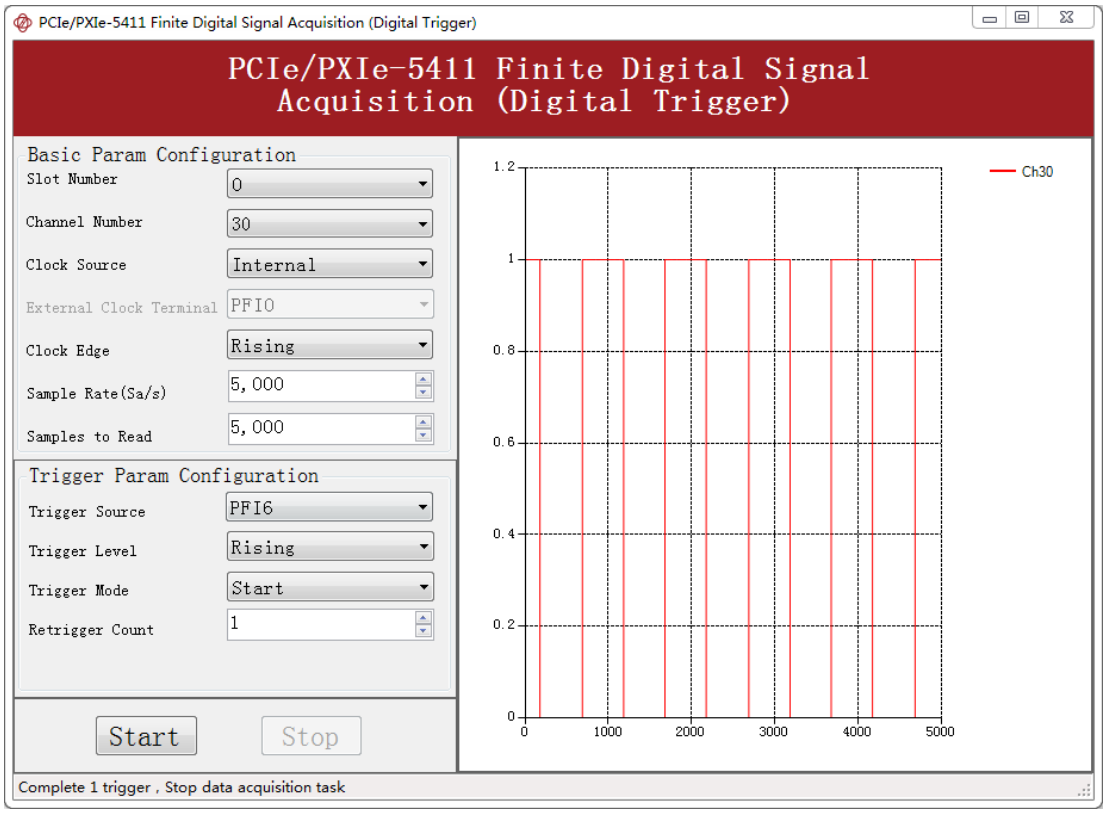

Figure 23

- Now change the **Trigger Mode** to **Reference** mode with **Pretrigger Samples** 100.

- A different result shows below:

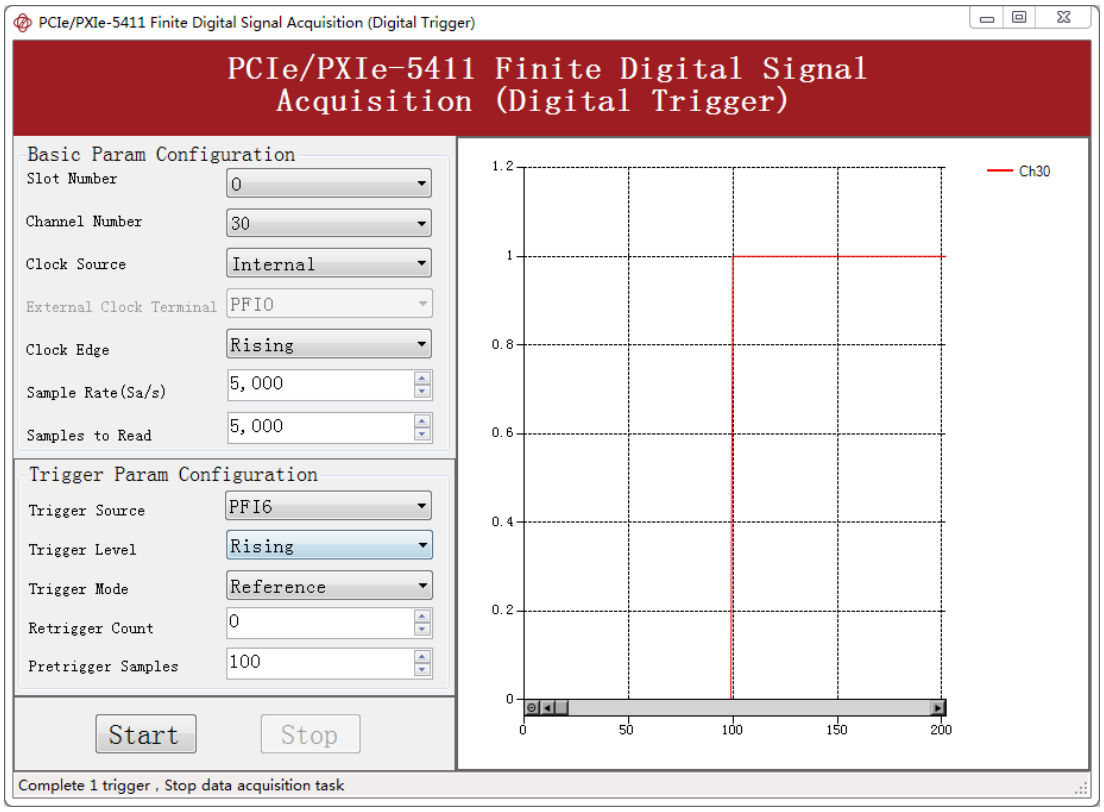

Figure 24

- You can see the data acquisition starts with 100 samples later than before due to the change of **Trigger Mode**.
- Now change the mode of trigger to *Retrigger* through giving **Retrigger Count** a number other than 0 and click **Start**. A message will appear in the lower left corner: “Complete the Nth trigger”.

Figure 25

- It shows the acquisition process after every trigger signal.

4.7 System Synchronization Interface（SSI）for PCIe Modules

The synchronization between PCIe modules are handled differently from the PXIe synchronization, it is implemented by the system synchronization interface (SSI). SSI is designed as a bidirectional bus and it can synchronize up to four PCIe modules. One PCIe module is designated as the master module and the other PCIe modules are designated as the slave modules.

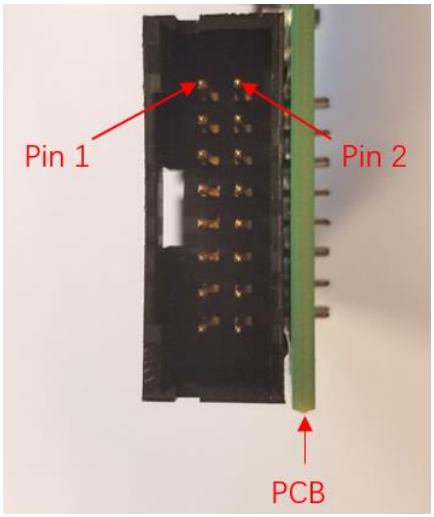

Figure 26 SSI Connector in PCIe-5411

Pin	Signal Name	Signal Name	Pin
1	PXI_TRIG0	GND	2
3	PXI_TRIG1	GND	4
5	PXI_TRIG2	GND	6
7	PXI_TRIG3	GND	8
9	PXI_TRIG4	GND	10
11	PXI_TRIG5	GND	12
13	PXI_TRIG6	GND	14
15	PXI_TRIG7	GND	16

Table 13 SSI Connector Pin Assignment for PCIe-5411

4.8 DIP Switch in PCIe-5411

PCIe-5411 series modules have a DIP switch. The card number can be adjusted manually by changing the DIP switch setting, which is used to identify the boards with different slot positions.

For example, if you want to set the card number to 3, you could turn the position 2 and 1 of the DIP switch to the ON position and the orthers to OFF. See below for details.

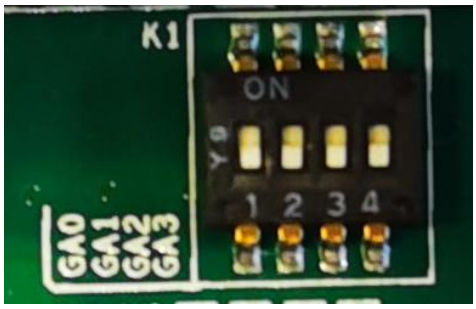

Figure 27 DIP Switch in PCIe-5411

	Position 4 (GA3)	Position 3 (GA2)	Position 2 (GA1)	Position 1 (GA0)
Slot 0	0	0	0	0
Slot 1	0	0	0	1
Slot 2	0	0	1	0
Slot 3	0	0	1	1
Slot 4	0	1	0	0
Slot 5	0	1	0	1
Slot 6	0	1	1	0
Slot 7	0	1	1	1
Slot 8	1	0	0	0
Slot 9	1	0	0	1
Slot 10	1	0	1	0
Slot 11	1	0	1	1
Slot 12	1	1	0	0
Slot 13	1	1	0	1
Slot 14	1	1	1	0
Slot 15	1	1	1	1
Note: OFF=0/ ON=1				

Table 14 Relationship between switch position and slot number

5. Using PCIe/PXIe-5411 in Other Software

While JYTEK's default application platform is Visual Studio, the programming language is C#, we recognize there are other platforms that are either becoming very popular or have been widely used in the data acquisition applications. Among them are Python, C++. This chapter explains how you can use PCIe/PXIe-5411 card using one of this software.

5.1 Python

JYTEK provides and supports a native Python driver for PCIe/PXIe-5411 cards. There are many different versions of Python. JYTEK has only tested in CPython version 3.5. There is no guarantee that JYTEK python drivers will work correctly with other versions of Python.

If you want to be our partner to support different Python platforms, please contact us.

5.2 C++

JYTEK internaly uses our C++ drivers to design the C# drivers. We recommend our customers to use C# drivers because C# platform deliver much better efficiency and performance in most situations. We also make our C++ drivers available. However, due to the limit of our resources, we do not actively support C++ drivers. You can download our C++ drivers from JYTEK's website. We welcome you report the bugs in our C++ drivers, but will not be able to guarantee that we can fix it within your expectation.

If you want to be our partner to support C++ drivers, please contact us.

6. About JYTEK

6.1 JYTEK China

Founded in June, 2016, JYTEK China is a leading Chinese test & measurement company, providing complete software and hardware products for the test and measurement industry. The company is a joint venture between Adlink Technologies and a group of experienced professionals form the industry. JYTEK independenly develop the software and hardware products and is entirely focused on the Chinese market. Our Shanghai headquarters and production service center have regular stocks to ensure timely supply; we have R&D centers in Xi'an and Chongqing to develop new products; we also have highly trained direct technical sales representatives in Shanghai, Beijing, Tianjin, Xi'an, Chengdu, Nanjing, Wuhan, Haerbin, and Changchun. We also have many patners who provide system level support in various cities.

6.2 JYTEK Hardware Products

According to JYTEK's agreement with our equity partner Adlink Technologies, JYTEK's hardware is manufactured by the state-of-art manufacturing facility located in Shanghai Zhangjiang Hi-Tech Park. Adlink has over 20 years of the world-class low-volumn and high-mix manufacturing expertise with ISO9001-2008, China 3C, UL, ROHS, TL9000, ISO-14001, ISO-13485 certifications. Its 30,000 square meters facilities and three high-speed Panasonic SMT production lines can produce 60,000 pieces boards/month; it also has full supply chain management - planning, sweeping, purchasing, warehousing and distribution. Adlink's manufacturing excellence ensures JYTEK's hardware has word-class manufacturing quality.

One core technical advantage is JYTEK's pursue for the basic and fundamental technology excellence. JYTEK China has developed a unique PCIe, PXIe, USB hardware driver architecture, FirmDrive, upon which many our future hardware will be based.

In addition to our own developed hardware, JYTEK also rebrands Adlink's PXI product lines. In addition, JYTEK has other rebranding agreements to increase our hardware coverage. It is our goal to provide the complete product coverage in PXI and PCI modular instrumentation and data acquisition.

6.3 JYTEK Software Platform

JYTEK has developed a complete software platform, SeeSharp Platform, for the test and measurement applications. We leverage the open sources communities to

provide the software tools. Our platform software is also open sourced and is free, thus lowering the cost of tests for our customers. We are the only domestic vendor to offer complete commercial software and hardware tools.

6.4 JYTEK Warranty and SupportServices

With our complete software and hardware products, JYTEK is able to provide technical and sales services to wide range of applications and customers. In most cases, our products are backed by a 1-year warranty. For technical consultation, pre-sale and after-sales support, please contact JYTEK of your country.

7. Statement

The hardware and software products described in this manual are provided by JYTEK China, or JYTEK in short.

This manual provides the product review, quick start, some driver interface explaination for PCIe/PXIe-6301 family of temperature sensor data acquisition cards. The manual is copyrighted by JYTEK.

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While we try to keep this manual up to date, there are factors beyond our control that may affect the accuracy of the manual. Please check the latest manual and product information from our website.

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